REMARKS

The claims are claims 1, 3, 10, 19 and 20.

Claims 1, 9, 10, 12, and 18 to 20 were rejected under 35 U.S.C. 103(a) as made obvious by the combination of Hansen et al U.S. Published Patent Application No. 2003/0110197 and Itoh U.S. Published Patent Application No. 2001/0009012.

Claims 1, 10, 19 and 20 recite subject matter not made obvious by the combination of Hansen et al and Itoh. Claims 1, 10, 19 and 20 recite "each of said first Booth decoder cell structurally the same as each of said second Booth decoder cell except that at least one of a first plurality of transistors of said first Booth decoder cell is constructed to have a width greater than a width of a corresponding one of a second plurality of transistors of said second Booth decoder cell" and "each of said first Wallace tree cell structurally the same as each of said second Wallace tree cell except that at least one of a first plurality of transistors of said first Wallace tree cell is constructed to have a width greater than a width of a corresponding one a second plurality of transistors of said second Wallace tree cell.". Hansen et al neither teaches a transistor difference in width of nor cells differing in any way. The FINAL REJECTION states at page 4, lines 10 to 15:

> "Hansen et al. fail to disclose at least one of the first Booth decoder cell as transistor is constructed to have a width greater than a width of a corresponding transistor of second Booth decoder cell as transistor. However, Itoh explicitly discloses at least one of the first Booth decoder cell as transistor is constructed to have a width greater than a width of a corresponding transistor of second Booth decoder cell as transistor (e.g. paragraph [0036] and [0042])."

The Applicants respectfully submit that Itoh fails to teach differing transistor widths as recited in claims 1, 10, 19 and 20. Itoh states at paragraph [0036]:

> "[0036] If the size of the component transistor (a ratio of a channel width to a channel length in the case of an MOS transistor) is increased to generate an output at high speed in each stage, the area of the multiplication array of the multiplication apparatus increases. Thus, the size of the component transistor is the minimum required size to increase integration degree. The third order partial product must be transmitted from the third order 4:2 addition circuit 6a to final addition circuit 7 over a distance of half the length of the multiplication array. A signal propagation delay during the transmission increases, whereby high speed multiplication cannot be achieved."

This portion of Itoh teaches selecting a transistor size at a minimum size to achieve the desired operational speed. Itoh fails to teach making two such transistor size selections for circuits of differing locations. Without teaching the differing selection of transistor size recited in claims 1, 10, 19 and 20, Itoh fails to add to the teaching of Hansen et al to make obvious this limitation. Accordingly, claims 1, 10, 19 and 20 are allowable over the combination of Hansen et al and Itoh.

Claims 1, 10, 19 and 20 recite further subject matter not made obvious by the combination of Hansen et al and Itoh. Claims 1, 10, 19 and 20 each recite at least one critical path. As pointed out by the Examiner, Hansen et al inherently includes such critical paths. Apparatus claims 1 and 10 each recite "wherein said at least one first Wallace tree cell and said at least one first Booth decoder cell are disposed on said at least one critical path; and wherein said at least one second Wallace tree cell and said at least one second Booth decoder cell are disposed on an electrical path not said at least one critical path and are not disposed on any of said at least one critical path." Method claims 19 and 20

similarly recite "disposing at least one first Wallace tree cell and at least one first Booth decoder cell on said at least one critical path; disposing at least one second Wallace tree cell and at least one second Booth decoder cell are on an electrical path not said at least one critical path; and not disposing any second Wallace tree cell or any second Booth decoder on any of said at least one critical path." Hansen et al fails to teach defining critical paths and the two types of cells used depend upon whether the cell is on such a critical path. Hansen et al likewise fails to teach that one type cell is used in critical paths and another type cell is used in paths not critical paths and not used in critical paths. The teaching of Itoh adds nothing to make this limitation obvious because Itoh fails to teach the recited critical path. Itoh likewise fails to teach constructing cells with differing transistor widths for differing locations within the circuit. Accordingly, claims 1, 10, 19 and 20 are allowable over the combination of Hansen et al and Itoh.

Paragraph 5 on page 5 of the FINAL REJECTION states that claims 3 and 12 are allowable but dependent upon a rejected base claim. The Applicants respectfully submit that the above arguments show that base claims 1 and 10 are allowable. Thus claims 3 and 12 are allowable.

The Applicants respectfully request entry and consideration of this amendment. Entry of this amendment is proper at this time because the amendment serves only to clarify subject matter previously recited. Thus no new search or reconsideration is required.

The Applicants respectfully submit that all the present claims are allowable for the reasons set forth above. Therefore early entry of this amendment, reconsideration and advance to issue are respectfully requested.

If the Examiner has any questions or other correspondence regarding this application, Applicants request that the Examiner contact Applicants' attorney at the below listed telephone number and address to facilitate prosecution.

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Respectfully submitted,

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